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EXAMINER	
THANGAVELU, KANDASAMY	
ART UNIT	**PAPER NUMBER**
2123	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/612,582	NARAHARA ET AL.
	Examiner	Art Unit
	Kandasamy Thangavelu	2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _30 December 2004_.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-30_ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-30_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _07 July 2000_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. This communication is in response to the Applicant's Amendments, mailed on December 30, 2004. Claims 1, 28 and 30 were amended. Claims 1-30 are pending. This office action is made final.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. §112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-30 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 1 states in part, "a transforming step of **transforming said instantaneous current amount into an instantaneous electric current** according to a predetermined rule related to said instantaneous current amount". The specification does not specify anywhere how **the instantaneous current amount is transformed into an instantaneous electric current** and what rules are used to transform the current amount into current.

Claim 28 states in part, "transforming means for **transforming said instantaneous electric current amount into an instantaneous electric current** according to a predetermined rule related to said instantaneous current amount". The specification does not specify anywhere how **the instantaneous current amount is transformed into an instantaneous electric current** and what rules are used to transform the current amount into current.

Claims rejected but not specifically addressed are rejected based on their dependency on rejected claims.

4. The following is a quotation of the second paragraph of 35 U.S.C. § 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 1 is rejected under 35 U.S.C. § 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are:

electromagnetic interference analyzing step of analyzing the amount of electromagnetic interference arising in an LSI on the basis of a signal output from the FFT processing step.

Such an essential step appears in Claim 28. Without such a step, the electromagnetic analysis method terminates with an FFT processing step and so is incomplete. It is not clear as to what is done with the results of FFT analysis.

The preamble of the claim states, "An electromagnetic interference analysis method for analyzing the amount of electromagnetic interference arising in an LSI by means of performing a gate level simulation'. Therefore, a step of electromagnetic interference analysis must follow the FFT processing step, to achieve the objective of the preamble.

6. Claims 2-15, 21-22 and 25-27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 2-15 and 25-27 state in part, "The electromagnetic interference analysis method as defined in claim 1, wherein **the modeling step** includes". There is insufficient antecedent basis for this limitation in these claims. Claim 1 does not refer to any modeling step.

Claims 21-22 state in part, "The electromagnetic interference analysis method as defined in claim 15, wherein **the modeling step includes**". There is insufficient antecedent basis for this limitation in these claims. Claim 15 refers to the modeling step of claim1, but claim 1 does not refer to any modeling step.

Claim Interpretations

7. In claim 1, "a transforming step of transforming said instantaneous current amount into an instantaneous electric current according to a predetermined rule related to said instantaneous current amount" has been interpreted as "a transforming step of transforming said instantaneous current amount into an instantaneous electric current **waveform** according to a predetermined rule related to said instantaneous current amount".

In claim 28, "transforming means for transforming said instantaneous electric current amount into an instantaneous electric current according to a predetermined rule related to said instantaneous current amount" has been interpreted as "transforming means for transforming said instantaneous electric current amount into an instantaneous electric current **waveform** according to a predetermined rule related to said instantaneous current amount".

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

9. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claims 1, 3-7, 14-17, 20, 24 and 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hayashi et al.** ("EMI- Noise analysis under ASIC design environment", ACM 1999) in view of **Zarkesh et al.** (U.S. Patent 6,212,665), and further in view of **Roethig** (U.S. Patent 5,835,380).

10.1 **Hayashi et al.** teaches EMI Noise analysis under ASIC design environment. Specifically, as per Claim 1, **Hayashi et al.** teaches an electromagnetic interference analysis method for analyzing the amount of electromagnetic interference arising in an LSI by means of performing a logic simulation using cell switching simulation (Page 16, CL1, Abstract; Page 16, CL2, Para 4; Page 16, CL2, Para 8, using cell information; Page 17, CL1, Para 1, switch-level simulator; Page 18, CL2, Para 3, input netlist, switching simulator; Para 4, logic simulation, each event, when the cell switches; Page 19, Fig. 12, logic simulation, cell switching; Page 19, CL2, Para 3, SPICE simulation, current/voltage waveforms, FFT transform and noise spectrum analysis); the method comprising:

an instantaneous current amount calculation step of calculating the amount of instantaneous electric current from event information, the information being produced when a change arises in a signal (Page 16, CL2, Para 1; Page 16, CL2, Para 3; Page 18, CL2, Para 4; Page 19, CL1, Fig 12; Page 19, CL2, Para 2); and

including the instance name of each cell in which the change has arisen, the name of the signal, a time at which the change has arisen, and transition information (Page 18, CL2, Para 4; Page 19, CL1, Fig 12; Page 19, CL2, Para 2; the event when cell switches is recorded in the logic simulation and the current waveforms of the area obtained; the simulation uses the netlist); and

an FFT processing step of subjecting to fast Fourier processing the information concerning a change in electric current, the information being calculated through the transforming step (Page 19, CL2, Para 3; Page 18, CL2, Para 4 to Page 19, CL1, Para 1; Page 16, CL2, Para 3; Page 16, CL2, Para 3).

Hayashi et al. does not expressly teach an electromagnetic interference analysis method for analyzing the amount of electromagnetic interference arising in an LSI by means of performing a gate level simulation. **Zarkesh et al.** teaches that the logic simulation performed by **Hayashi et al.** is gate level simulation and therefore involves an electromagnetic interference analysis method for analyzing the amount of electromagnetic interference arising in an LSI by means of performing a gate level simulation (Abstract, L7; CL1, L41-47), because netlist is a gate-level netlist (Abstract, L7); and the term cell includes transistors, gates such as NAND or OR gate and macro circuit portions such as adder or flip-flop (CL1, L41-47) and therefore, the cell level simulation implies gate-level simulation. It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to interpret the method of **Hayashi et al.** involving the cell level simulation as gate level simulation using the description of **Zarkesh et al.** The artisan would have been motivated because netlist is a gate-level netlist; and the term cell includes transistors, gates such as NAND or OR gate and macro circuit portions such as adder or flip-flop and therefore, the cell level simulation implies gate-level simulation.

Hayashi et al. does not expressly teach a transforming step of transforming the instantaneous current amount into an instantaneous electric current according to a predetermined rule related to the instantaneous current amount. **Roethig** teaches a transforming step of

transforming the instantaneous current amount into an instantaneous electric current according to a predetermined rule related to the instantaneous current amount (Abstract, L1-2 and L7-12; CL3, L25-30; CL5, L13-33; CL6, L17-22), because by decomposing the cell currents, the circuit designer can perform more accurate power analysis and modify the design to better accommodate the power consumption by changing the loading of the cell to reduce the load current (CL3, L16-22); and as per **Hayashi et al.**, by performing fast Fourier transformation for the current waveforms, EMI noise spectrum can be obtained (Page 19, CL2, Para 2 & 3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Roethig** that included a transforming step of transforming the instantaneous current amount into an instantaneous electric current according to a predetermined rule related to the instantaneous current amount. The artisan would have been motivated because by decomposing the cell currents, the circuit designer could perform more accurate power analysis and modify the design to better accommodate the power consumption by changing the loading of the cell to reduce the load current; and by performing fast Fourier transformation for the current waveforms, EMI noise spectrum could be obtained.

10.2 As per Claim 3, **Hayashi et al., Zarkesh et al.** and **Roethig** teach the method of claim 1. **Hayashi et al.** teaches that the FFT processing step includes a step of subjecting to FFT processing information concerning a change in current, the information being calculated in the rectangular waveform modeling step (Page 19, CL2, Para 3).

Hayashi et al. does not expressly teach that the modeling step includes a rectangular waveform modeling step of modeling the instantaneous current as a rectangular waveform whose

height is calculated from information for each event such that the area of the rectangular waveform becomes equal to the amount of electric current of each event. **Roethig** teaches that the modeling step includes a rectangular waveform modeling step of modeling the instantaneous current as a rectangular waveform whose height is calculated from information for each event such that the area of the rectangular waveform becomes equal to the amount of electric current of each event (Abstract, L1-2 and L7-12; CL3, L25-30; CL5, L13-33; CL6, L17-22), because rectangular waveforms represent the Vdd and Vss currents consumed by the cells (CL5, L28-29); and by decomposing the cell currents, the circuit designer can perform more accurate power analysis and modify the design to better accommodate the power consumption by changing the loading of the cell to reduce the load current (CL3, L16-22); and as per **Hayashi et al.**, by performing fast Fourier transformation for the current waveforms, EMI noise spectrum can be obtained (Page 19, CL2, Para 2 & 3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Roethig** that included the modeling step including a rectangular waveform modeling step of modeling the instantaneous current as a rectangular waveform whose height was calculated from information for each event such that the area of the rectangular waveform became equal to the amount of electric current of each event; and the FFT processing step including the information calculated in the rectangular waveform modeling step. The artisan would have been motivated because rectangular waveforms would represent the Vdd and Vss currents consumed by the cells; and by decomposing the cell currents, the circuit designer could perform more accurate power analysis and modify the design to better accommodate the power consumption by

changing the loading of the cell to reduce the load current; and by performing fast Fourier transformation for the current waveforms, EMI noise spectrum could be obtained.

10.3 As per Claim 4, **Hayashi et al., Zarkesh et al.** and **Roethig** teach the method of claim 1. **Hayashi et al.** teaches that the FFT processing step includes a step of subjecting to FFT processing information concerning a change in current, the information being calculated in the geometrically-similar rectangular waveform modeling step (Page 19, CL2, Para 3).

Hayashi et al. does not expressly teach that the modeling step includes a rectangular waveform modeling step of modeling the instantaneous current as a geometrically-similar rectangular waveform whose height is calculated from information for each event such that the area of the rectangular waveform becomes equal to the amount of electric current of each event. **Roethig** teaches that the modeling step includes a rectangular waveform modeling step of modeling the instantaneous current as a geometrically-similar rectangular waveform whose height is calculated from information for each event such that the area of the rectangular waveform becomes equal to the amount of electric current of each event (Abstract, L1-2 and L7-12; CL3, L25-30; CL5, L13-33; CL6, L17-22), because rectangular waveforms represent the Vdd and Vss currents consumed by the cells (CL5, L28-29); and by decomposing the cell currents, the circuit designer can perform more accurate power analysis and modify the design to better accommodate the power consumption by changing the loading of the cell to reduce the load current (CL3, L16-22); and as per **Hayashi et al.**, by performing fast Fourier transformation for the current waveforms, EMI noise spectrum can be obtained (Page 19, CL2, Para 2 & 3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to

modify the method of **Hayashi et al.** with the method of **Roethig** that included the modeling step including a rectangular waveform modeling step of modeling the instantaneous current as a geometrically-similar rectangular waveform whose height was calculated from information for each event such that the area of the rectangular waveform became equal to the amount of electric current of each event; and the FFT processing step including the information calculated in the rectangular waveform modeling step. The artisan would have been motivated because rectangular waveforms would represent the Vdd and Vss currents consumed by the cells; and by decomposing the cell currents, the circuit designer could perform more accurate power analysis and modify the design to better accommodate the power consumption by changing the loading of the cell to reduce the load current; and by performing fast Fourier transformation for the current waveforms, EMI noise spectrum could be obtained.

10.4 As per Claim 5, **Hayashi et al., Zarkesh et al.** and **Roethig** teach the method of claim 1. **Hayashi et al.** teaches subjecting to FFT processing the information concerning a change in electric current calculated in the rectangular waveform modeling step (Page 19, CL2, Para 3)

Hayashi et al. does not expressly teach that the modeling step includes a rectangular waveform modeling step of calculating the instantaneous electric current from each event information, and a step of modeling the instantaneous current as a rectangular waveform through use of the amount of electric current and a table representing the relationship between the width and height of a rectangular waveform. **Roethig** teaches that the modeling step includes a rectangular waveform modeling step of calculating the instantaneous electric current from each event information, and a step of modeling the instantaneous current as a rectangular waveform

through use of the amount of electric current and a table representing the relationship between the width and height of a rectangular waveform (Abstract, L1-2 and L7-12; CL3, L25-30; CL5, L13-33; CL6, L17-22; CL3, L23-25), because rectangular waveforms represent the Vdd and Vss currents consumed by the cells (CL5, L28-29); and by decomposing the cell currents, the circuit designer can perform more accurate power analysis and modify the design to better accommodate the power consumption by changing the loading of the cell to reduce the load current (CL3, L16-22); and as per **Hayashi et al.**, by performing fast Fourier transformation for the current waveforms, EMI noise spectrum can be obtained (Page 19, CL2, Para 2 & 3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Roethig** that included the modeling step including a rectangular waveform modeling step of calculating the instantaneous electric current from each event information, and a step of modeling the instantaneous current as a rectangular waveform through use of the amount of electric current; and subjecting to FFT processing the information concerning a change in electric current calculated in the rectangular waveform modeling step. The artisan would have been motivated because rectangular waveforms would represent the Vdd and Vss currents consumed by the cells; and by decomposing the cell currents, the circuit designer could perform more accurate power analysis and modify the design to better accommodate the power consumption by changing the loading of the cell to reduce the load current; and by performing fast Fourier transformation for the current waveforms, EMI noise spectrum could be obtained.

10.5 As per Claim 6, **Hayashi et al., Zarkesh et al.** and **Roethig** teach the method of claim 1. **Hayashi et al.** teaches the modeling step includes a step of calculating the instantaneous electric current from information for each event (Page 16, CL2, Para 1; Page 16, CL2, Para 3; Page 18, CL2, Para 4; Page 19, CL1, Fig 12; Page 19, CL2, Para 2); and a modeling step of modeling the instantaneous current through use of a slew in input waveform (Page 18, CL2, Para 4), to thereby subject to FFT processing the information concerning a change in electric current calculated in the rectangular waveform modeling step (Page 19, CL2, Para 3)

Hayashi et al. does not expressly teach a rectangular waveform modeling step of modeling the instantaneous current as a rectangular waveform through use of a table representing the relationship between the width and height of a rectangular waveform. **Roethig** teaches a rectangular waveform modeling step of modeling the instantaneous current as a rectangular waveform through use of a table representing the relationship between the width and height of a rectangular waveform (Abstract, L1-2 and L7-12; CL3, L25-30; CL5, L13-33; CL6, L17-22; CL3, L23-25), because rectangular waveforms represent the Vdd and Vss currents consumed by the cells (CL5, L28-29); and by decomposing the cell currents, the circuit designer can perform more accurate power analysis and modify the design to better accommodate the power consumption by changing the loading of the cell to reduce the load current (CL3, L16-22); and as per **Hayashi et al.**, by performing fast Fourier transformation for the current waveforms, EMI noise spectrum can be obtained (Page 19, CL2, Para 2 & 3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Roethig** that included a rectangular waveform modeling step of modeling the instantaneous current as a rectangular waveform through use of a table representing

the relationship between the width and height of a rectangular waveform. The artisan would have been motivated because rectangular waveforms would represent the Vdd and Vss currents consumed by the cells; and by decomposing the cell currents, the circuit designer could perform more accurate power analysis and modify the design to better accommodate the power consumption by changing the loading of the cell to reduce the load current; and by performing fast Fourier transformation for the current waveforms, EMI noise spectrum could be obtained.

10.6 As per Claim 7, **Hayashi et al., Zarkesh et al.** and **Roethig** teach the method of claim 1. **Hayashi et al.** teaches the modeling step includes a step of calculating the instantaneous electric current from information for each event (Page 16, CL2, Para 1; Page 16, CL2, Para 3; Page 18, CL2, Para 4; Page 19, CL1, Fig 12; Page 19, CL2, Para 2); and a modeling step of modeling the instantaneous current through use of an output load capacitance (Page 18, CL2, Para 4), to thereby subject to FFT processing the information concerning a change in electric current calculated in the rectangular waveform modeling step (Page 19, CL2, Para 3)

Hayashi et al. does not expressly teach a rectangular waveform modeling step of modeling the instantaneous current as a rectangular waveform through use of a table representing the relationship between the width and height of a rectangular waveform. **Roethig** teaches a rectangular waveform modeling step of modeling the instantaneous current as a rectangular waveform through use of a table representing the relationship between the width and height of a rectangular waveform (Abstract, L1-2 and L7-12; CL3, L25-30; CL5, L13-33; CL6, L17-22; CL3, L23-25), because rectangular waveforms represent the Vdd and Vss currents consumed by the cells (CL5, L28-29); and by decomposing the cell currents, the circuit designer can perform

more accurate power analysis and modify the design to better accommodate the power consumption by changing the loading of the cell to reduce the load current (CL3, L16-22); and as per **Hayashi et al.**, by performing fast Fourier transformation for the current waveforms, EMI noise spectrum can be obtained (Page 19, CL2, Para 2 & 3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Roethig** that included a rectangular waveform modeling step of modeling the instantaneous current as a rectangular waveform through use of a table representing the relationship between the width and height of a rectangular waveform. The artisan would have been motivated because rectangular waveforms would represent the Vdd and Vss currents consumed by the cells; and by decomposing the cell currents, the circuit designer could perform more accurate power analysis and modify the design to better accommodate the power consumption by changing the loading of the cell to reduce the load current; and by performing fast Fourier transformation for the current waveforms, EMI noise spectrum could be obtained.

10.7 As per Claim 14, **Hayashi et al., Zarkesh et al.** and **Roethig** teach the method of claim 1. **Hayashi et al.** does not expressly teach that the modeling step includes a step of modeling the amount of instantaneous electric current while separating the same into a short circuit electric current component and a charge current component. **Zarkesh et al.** teaches that the modeling step includes a step of modeling the amount of instantaneous electric current while separating the same into a short circuit electric current component and a charge current component (Abstract, L1-5 and L11-19; Fig. 5E; CL2, L59-64; CL7, L1-8), as the energy dissipation caused by switching activity is a function of charge /discharge current and short circuit current for a given

cell of specified characteristics (CL7, L1-3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Zarkesh et al.** that included the modeling step including a step of modeling the amount of instantaneous electric current while separating the same into a short circuit electric current component and a charge current component. The artisan would have been motivated because the energy dissipation caused by switching activity would be a function of charge /discharge current and short circuit current for a given cell of specified characteristics.

10.8 As per Claim 15, **Hayashi et al., Zarkesh et al.** and **Roethig** teach the method of claim 1. **Hayashi et al.** teaches that the FFT processing step includes a step of subjecting to FFT processing information concerning a change in current, the information being calculated in the rectangular waveform modeling step (Page 19, CL2, Para 3).

Hayashi et al. does not expressly teach that the modeling step includes a calculation step of calculating the height of a rectangular waveform from a library in which peak currents of cells are characterized according to the type of cell, and a rectangular waveform modeling step of modeling the amount of instantaneous electric current as a rectangular waveform, the peak current calculated in the calculation step being taken as the height of the rectangular waveform and the area of the rectangular waveform being equal to the amount of electric current of each event. **Roethig** teaches that the modeling step includes a calculation step of calculating the height of a rectangular waveform from a library in which peak currents of cells are characterized according to the type of cell, and a rectangular waveform modeling step of modeling the amount of instantaneous electric current as a rectangular waveform, the peak current calculated in the

calculation step being taken as the height of the rectangular waveform and the area of the rectangular waveform being equal to the amount of electric current of each event (Abstract, L1-2 and L7-12; CL3, L25-30; CL5, L13-33; CL6, L17-22; CL3, L23-25), because rectangular waveforms represent the Vdd and Vss currents consumed by the cells (CL5, L28-29); and by decomposing the cell currents, the circuit designer can perform more accurate power analysis and modify the design to better accommodate the power consumption by changing the loading of the cell to reduce the load current (CL3, L16-22); and as per **Hayashi et al.**, by performing fast Fourier transformation for the current waveforms, EMI noise spectrum can be obtained (Page 19, CL2, Para 2 & 3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Roethig** that included the modeling step including a calculation step of calculating the height of a rectangular waveform from a library in which peak currents of cells were characterized according to the type of cell, and a rectangular waveform modeling step of modeling the amount of instantaneous electric current as a rectangular waveform, the peak current calculated in the calculation step being taken as the height of the rectangular waveform and the area of the rectangular waveform being equal to the amount of electric current of each event. The artisan would have been motivated because rectangular waveforms would represent the Vdd and Vss currents consumed by the cells; and by decomposing the cell currents, the circuit designer could perform more accurate power analysis and modify the design to better accommodate the power consumption by changing the loading of the cell to reduce the load current; and by performing fast Fourier transformation for the current waveforms, EMI noise spectrum could be obtained.

10.9 As per Claim 16, **Hayashi et al., Zarkesh et al.** and **Roethig** teach the method of claim 15. **Hayashi et al.** also teaches that the calculation step includes a step of calculating a peak current for each cell from information concerning a slew in the cell, by reference to a library in which the relationship between a slew in input waveform and a peak current is characterized in the form of a table according to the type of cell (Page 18, CL2, Para 4).

10.10 As per Claim 17, **Hayashi et al., Zarkesh et al.** and **Roethig** teach the method of claim 15. **Hayashi et al.** also teaches that the calculation step includes a step of calculating a peak current for each cell from information concerning a load capacitance of a cell, by reference to a library in which the relationship between a load capacitance and a peak current is characterized in the form of a table according to the type of cell (Page 18, CL2, Para 4).

10.11 As per Claim 20, **Hayashi et al., Zarkesh et al.** and **Roethig** teach the method of claim 15. **Hayashi et al.** does not expressly teach that the calculation step includes a step of calculating the height of a rectangular waveform through use of a library in which peak currents are characterized in consideration of the state of an input signal. **Roethig** teaches that the calculation step includes a step of calculating the height of a rectangular waveform through use of a library in which peak currents are characterized in consideration of the state of an input signal (Abstract, L1-2 and L7-12; CL3, L25-30; CL5, L13-33; CL6, L17-22; CL3, L23-25), because rectangular waveforms represent the Vdd and Vss currents consumed by the cells (CL5, L28-29); and by decomposing the cell currents, the circuit designer can perform more accurate power analysis and modify the design to better accommodate the power consumption by

changing the loading of the cell to reduce the load current (CL3, L16-22); and as per **Hayashi et al.**, by performing fast Fourier transformation for the current waveforms, EMI noise spectrum can be obtained (Page 19, CL2, Para 2 & 3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Roethig** that included the calculation step including a step of calculating the height of a rectangular waveform through use of a library in which peak currents were characterized in consideration of the state of an input signal. The artisan would have been motivated because rectangular waveforms would represent the Vdd and Vss currents consumed by the cells; and by decomposing the cell currents, the circuit designer could perform more accurate power analysis and modify the design to better accommodate the power consumption by changing the loading of the cell to reduce the load current; and by performing fast Fourier transformation for the current waveforms, EMI noise spectrum could be obtained.

10.12 As per Claim 24, **Hayashi et al., Zarkesh et al.** and **Roethig** teach the method of claim 15. **Hayashi et al.** does not expressly teach that the calculation step includes a step of modeling the amount of instantaneous electric current while separating the same into a short circuit electric current component and a charge current component. **Zarkesh et al.** teaches that the calculation step includes a step of modeling the amount of instantaneous electric current while separating the same into a short circuit electric current component and a charge current component (Abstract, L1-5 and L11-19; Fig. 5E; CL2, L59-64; CL7, L1-8), as the energy dissipation caused by switching activity is a function of charge /discharge current and short circuit current for a given cell of specified characteristics (CL7, L1-3). It would have been obvious to one of ordinary skill

in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Zarkesh et al.** that included the calculation step including a step of modeling the amount of instantaneous electric current while separating the same into a short circuit electric current component and a charge current component. The artisan would have been motivated because the energy dissipation caused by switching activity would be a function of charge /discharge current and short circuit current for a given cell of specified characteristics.

10.13 As per Claim 28, **Hayashi et al.** teaches an electromagnetic interference analysis system for analyzing the amount of electromagnetic interference arising in an LSI by means of performing a logic simulation using cell switching simulation (Page 16, CL1, Abstract; Page 16, CL2, Para 4; Page 16, CL2, Para 8, using cell information; Page 17, CL1, Para 1, switch-level simulator; Page 18, CL2, Para 3, input netlist, switching simulator; Para 4, logic simulation, each event, when the cell switches; Page 19, Fig. 12, logic simulation, cell switching; Page 19, CL2, Para 3, SPICE simulation, current/voltage waveforms, FFT transform and noise spectrum analysis); the system comprising:

a logic simulator (Page 18, CL2, Para 4);

computation means which is connected to the logic simulator and calculates the amount of instantaneous electric current from event information, the information being produced when a change arises in a signal (Page 16, CL2, Para 1; Page 16, CL2, Para 3; Page 18, CL2, Para 4; Page 19, CL1, Fig 12; Page 19, CL2, Para 2); and

including the instance name of each cell in which the change has arisen, the name of the signal, a time at which the change has arisen, and transition information (Page 18, CL2, Para 4;

Page 19, CL1, Fig 12; Page 19, CL2, Para 2; the event when cell switches is recorded in the logic simulation and the current waveforms of the area obtained; the simulation uses the netlist); and

fast Fourier (FFT) conversion means for subjecting to fast Fourier processing the information concerning a change in electric current, the information being calculated through the transforming means (Page 19, CL2, Para 3; Page 18, CL2, Para 4 to Page 19, CL1, Para 1; Page 16, CL2, Para 3; Page 16, CL2, Para 3);

thereby analyzing the amount of electromagnetic interference arising in an LSI on the basis of a signal output from the FFT conversion means (Page 19, CL2, Para 3; Page 16, CL2, Para 3; Page 16, CL2, Para 3).

Hayashi et al. does not expressly teach an electromagnetic interference analysis system for analyzing the amount of electromagnetic interference arising in an LSI by means of performing a gate level simulation. **Zarkesh et al.** teaches that the logic simulation performed by **Hayashi et al.** is gate level simulation and therefore involves an electromagnetic interference analysis method for analyzing the amount of electromagnetic interference arising in an LSI by means of performing a gate level simulation (Abstract, L7; CL1, L41-47), because netlist is a gate-level netlist (Abstract, L7); and the term cell includes transistors, gates such as NAND or OR gate and macro circuit portions such as adder or flip-flop (CL1, L41-47) and therefore, the cell level simulation implies gate-level simulation. It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to interpret the system of **Hayashi et al.** involving the cell level simulation as gate level simulation using the description of **Zarkesh et al.** The artisan would have been motivated because netlist is a gate-level netlist; and the term

cell includes transistors, gates such as NAND or OR gate and macro circuit portions such as adder or flip-flop and therefore, the cell level simulation implies gate-level simulation.

Hayashi et al. does not expressly teach transforming means for transforming the instantaneous current amount into an instantaneous electric current according to a predetermined rule related to the instantaneous current amount. **Roethig** teaches transforming means for transforming the instantaneous current amount into an instantaneous electric current according to a predetermined rule related to the instantaneous current amount (Abstract, L1-2 and L7-12; CL3, L25-30; CL5, L13-33; CL6, L17-22), because by decomposing the cell currents, the circuit designer can perform more accurate power analysis and modify the design to better accommodate the power consumption by changing the loading of the cell to reduce the load current (CL3, L16-22); and as per **Hayashi et al.**, by performing fast Fourier transformation for the current waveforms, EMI noise spectrum can be obtained (Page 19, CL2, Para 2 & 3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Roethig** that included transforming means for transforming the instantaneous current amount into an instantaneous electric current according to a predetermined rule related to the instantaneous current amount. The artisan would have been motivated because by decomposing the cell currents, the circuit designer could perform more accurate power analysis and modify the design to better accommodate the power consumption by changing the loading of the cell to reduce the load current; and by performing fast Fourier transformation for the current waveforms, EMI noise spectrum could be obtained.

10.14 As per Claim 29, **Hayashi et al., Zarkesh et al.** and **Roethig** teach the method of claim 1.. **Hayashi et al.** does not expressly teach the method further comprising the step of providing a gate level logic simulation. **Zarkesh et al.** teaches the method further comprising the step of providing a gate level logic simulation (CL1, L40-47), as the netlist used is a gate-level netlist (Abstract, L7) and a cell simulator includes a gate level simulator, since a cell could be a gate (CL1, L40-47). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to interpret the method of **Hayashi et al.** to include the gate level simulation of **Zarkesh et al.** The artisan would have been motivated because the netlist used would be a gate-level netlist and a cell simulator would include a gate level simulator, since a cell could be a gate.

10.15 As per Claim 30, **Hayashi et al., Zarkesh et al.** and **Roethig** teach the system of claim 28. **Hayashi et al.** does not expressly teach the system further comprising the step of providing a gate level logic simulation. **Zarkesh et al.** teaches the system further comprising the step of providing a gate level logic simulation (CL1, L40-47), as the netlist used is a gate-level netlist (Abstract, L7) and a cell simulator includes a gate level simulator, since a cell could be a gate (CL1, L40-47). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to interpret the method of **Hayashi et al.** to include the gate level simulation of **Zarkesh et al.** The artisan would have been motivated because the netlist used would be a gate-level netlist and a cell simulator would include a gate level simulator, since a cell could be a gate.

11. Claims 2, 11, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hayashi et al.** ("EMI- Noise analysis under ASIC design environment", ACM 1999) in view of **Zarkesh et al.** (U.S. Patent 6,212,665), and further in view of **Roethig** (U.S. Patent 5,835,380) and **Chen et al.** ("Power supply Noise analysis methodology for Deep-submicron VLSI chip design", ACM 1997).

11.1 As per Claim 2, **Hayashi et al., Zarkesh et al.** and **Roethig** teach the method of claim 1. **Hayashi et al.** teaches that the FFT processing step includes a step of subjecting to FFT processing information concerning a change in current (Page 19, CL2, Para 3).

Hayashi et al. does not expressly teach that the modeling step includes an averaging step of averaging the instantaneous current over a certain discrete width; and the information concerning a change in current being produced by the averaging step. **Chen et al.** teaches that the modeling step includes an averaging step of averaging the instantaneous current over a certain discrete width (Page 3, CL1, Para 3 to Page 3, CL2, Para 6); and the information concerning a change in current being produced by the averaging step (Page 3, CL1, Para 3), as a triangular or trepeziodal current waveform, which is a simpler form of the piecewise linear current model can be derived from the total average current, the piecewise linear current models mimicing the waveforms of the actual circuits (Page 3, CL1, Para 3); and as per **Hayashi et al.**, using the power network and switching current waveform data, SPICE simulation can be performed and current/voltage waveforms obtained; by performing fast Fourier transformation for the current waveforms, EMI noise spectrum can be obtained (Page 19, CL2, Para 2 & 3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to

modify the method of **Hayashi et al.** with the method of **Chen et al.** that included the modeling step including an averaging step of averaging the instantaneous current over a certain discrete width; and the information concerning a change in current being produced by the averaging step. The artisan would have been motivated because a triangular or trepeziodal current waveform, which would be a simpler form of the piecewise linear current model could be derived from the total average current, the piecewise linear current models mimicing the waveforms of the actual circuits; that would allow obtaining the switching current waveform as a function of input slew and output load; using the power network and switching current waveform data, SPICE simulation could be performed and current/voltage waveforms obtained; by performing fast Fourier transformation for the current waveforms, EMI noise spectrum could be obtained.

11.2 As per Claim 11, **Hayashi et al., Zarkesh et al.** and **Roethig** teach the method of claim 1. **Hayashi et al.** teaches that the modeling step includes a triangular waveform modeling step of modeling the instantaneous current as a triangular waveform (Page 19, CL1, Para 1; Fig 10); and that the FFT processing step includes a step of subjecting to FFT processing information concerning a change in current, the information being calculated in the triangular waveform modeling step (Page 19, CL2, Para 3).

Hayashi et al. does not expressly teach that triangular waveform has a given width and whose height is calculated for each event information such that the amount of instantaneous electric current becomes equal to the area of the triangular waveform. **Chen et al.** teaches that triangular waveform has a given width and whose height is calculated for each event information such that the amount of instantaneous electric current becomes equal to the area of the triangular

waveform (Page 3, CL1, Para 3 to Page 3, CL2, Para 6), as a triangular or trepeziodal current waveform, which is a simpler form of the piecewise linear current model can be derived from the total average current, the piecewise linear current models mimicing the waveforms of the actual circuits (Page 3, CL1, Para 3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Chen et al.** that included triangular waveform having a given width and whose height would be calculated for each event information such that the amount of instantaneous electric current became equal to the area of the triangular waveform. The artisan would have been motivated because a triangular or trepeziodal current waveform, which would be a simpler form of the piecewise linear current model could be derived from the total average current, the piecewise linear current models mimicing the waveforms of the actual circuits.

11.3 As per Claim 25, **Hayashi et al., Zarkesh et al.** and **Roethig** teach the method of claim 1. **Hayashi et al.** teaches that the modeling step includes a triangular waveform modeling step of modeling the instantaneous current as a triangular waveform (Page 19, CL1, Para 1; Fig 10) in consideration of slew information (i.e., an output slew) for an output terminal of a cell (Page 18, CL2, Para 4). **Hayashi et al.** teaches that the FFT processing step includes a step of subjecting to FFT processing information concerning a change in current, the information being calculated in the triangular waveform modeling step (Page 19, CL2, Para 3).

Hayashi et al. does not expressly teach that triangular waveform width is calculated from each event information such that the area of the triangular waveform becomes equal to the amount of electric current of each event, the height of the triangular waveform being calculated

on the basis of the width. **Chen et al.** teaches that triangular waveform width is calculated from each event information such that the area of the triangular waveform becomes equal to the amount of electric current of each event, the height of the triangular waveform being calculated on the basis of the width (Page 3, CL1, Para 3 to Page 3, CL2, Para 6), as a triangular or trepeziodal current waveform, which is a simpler form of the piecewise linear current model can be derived from the total average current, the piecewise linear current models mimicing the waveforms of the actual circuits (Page 3, CL1, Para 3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Chen et al.** that included triangular waveform width being calculated from each event information such that the area of the triangular waveform became equal to the amount of electric current of each event, the height of the triangular waveform being calculated on the basis of the width. The artisan would have been motivated because a triangular or trepeziodal current waveform, which would be a simpler form of the piecewise linear current model could be derived from the total average current, the piecewise linear current models mimicing the waveforms of the actual circuits.

11.4 As per Claim 26, **Hayashi et al., Zarkesh et al.** and **Roethig** teach the method of claim 1. **Hayashi et al.** teaches that the modeling step includes means of multiplying the amount of instantaneous electric current by a coefficient corresponding to the state of an event of a cell, in consideration of whether the event of the cell is in a rising state or a falling state (Page 18, CL2, Para 4 to Page 19, CL1, Para 1; Fig 10).

Hayashi et al. does not expressly teach that the modeling step includes a triangular height calculation step of calculating the height of a triangular waveform such that the area of the triangular waveform becomes equal to the amount of electric current of each event. **Chen et al.** teaches that the modeling step includes a triangular height calculation step of calculating the height of a triangular waveform such that the area of the triangular waveform becomes equal to the amount of electric current of each event (Page 3, CL1, Para 3 to Page 3, CL2, Para 6), as a triangular or trepeziodal current waveform, which is a simpler form of the piecewise linear current model can be derived from the total average current, the piecewise linear current models mimicing the waveforms of the actual circuits (Page 3, CL1, Para 3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Chen et al.** that included the modeling step including a triangular height calculation step of calculating the height of a triangular waveform such that the area of the triangular waveform becomes equal to the amount of electric current of each event. The artisan would have been motivated because a triangular or trepeziodal current waveform, which would be a simpler form of the piecewise linear current model could be derived from the total average current, the piecewise linear current models mimicing the waveforms of the actual circuits.

12. Claims 8-10 and 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hayashi et al.** ("EMI- Noise analysis under ASIC design environment", ACM 1999) in view of **Zarkesh et al.** (U.S. Patent 6,212,665), and further in view of **Roethig** (U.S. Patent 5,835,380) and **Kuwano et al.** (U.S. Patent 6,253,354).

12.1 As per Claim 8, **Hayashi et al.**, **Zarkesh et al.** and **Roethig** teach the method of claim 1. **Hayashi et al.** teaches that the modeling step includes the resistance of a power line and correcting the amount of instantaneous electric current of each cell for each event, on the basis of the relationship between the drop in voltage and the amount of instantaneous electric current (Page 19, CL1, Para 2; Page 18, CL1, Para 6 to CL2, Para 1).

Hayashi et al. does not expressly teach calculating a drop in voltage from the amount of electric current flowing in each cell and the resistance of a power line. **Kuwano et al.** teaches calculating a drop in voltage from the amount of electric current flowing in each cell and the resistance of a power line (CL2, L29-33), as that would allow analyzing the variations in the source voltage of a semiconductor device without test patterns (CL1, L9-10). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Kuwano et al.** that included calculating a drop in voltage from the amount of electric current flowing in each cell and the resistance of a power line. The artisan would have been motivated because that would allow analyzing the variations in the source voltage of a semiconductor device without test patterns.

12.2 As per Claim 9, **Hayashi et al.**, **Zarkesh et al.** and **Roethig** teach the method of claim 1. **Hayashi et al.** teaches that the modeling step includes the resistance of a power line, and the capacitance of an on-chip capacitor and correcting the amount of instantaneous electric current of each cell for each event, on the basis of the relationship between the drop in voltage and the

amount of instantaneous electric current (Page 19, CL1, Para 2; Page 17, CL1, Para 3 to Page 18, CL2, Para 1; Page 16, CL2, Para 8; Page 18, CL2, Fig 8).

Hayashi et al. does not expressly teach calculating a drop in voltage from the amount of electric current flowing in each cell and the resistance of a power line, and the capacitance of an on-chip capacitor. **Kuwano et al.** teaches calculating a drop in voltage from the amount of electric current flowing in each cell and the resistance of a power line, and the capacitance of an on-chip capacitor (CL2, L29-33), as that would allow analyzing the variations in the source voltage of a semiconductor device without test patterns (CL1, L9-10). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Kuwano et al.** that included calculating a drop in voltage from the amount of electric current flowing in each cell and the resistance of a power line, and the capacitance of an on-chip capacitor. The artisan would have been motivated because that would allow analyzing the variations in the source voltage of a semiconductor device without test patterns.

12.3 As per Claim 10, **Hayashi et al., Zarkesh et al.** and **Roethig** teach the method of claim 1. **Hayashi et al.** teaches that the modeling step includes a step of transiently analyzing a power RC of each cell and a cell power source, and a correction step of correcting the amount of instantaneous electric current of each cell for each event, on the basis of the relationship between the drop in voltage and the amount of instantaneous electric current (Page 19, CL1, Para 2; Page 17, CL1, Para 3 to Page 18, CL2, Para 1; Page 16, CL2, Para 8; Page 18, CL2, Fig 8).

Hayashi et al. does not expressly teach accurately calculating a drop in voltage. **Kuwano et al.** teaches accurately calculating a drop in voltage (CL2, L29-33), as that would allow analyzing the variations in the source voltage of a semiconductor device without test patterns (CL1, L9-10). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Kuwano et al.** that included accurately calculating a drop in voltage. The artisan would have been motivated because that would allow analyzing the variations in the source voltage of a semiconductor device without test patterns.

12.4 As per Claim 21, **Hayashi et al., Zarkesh et al.** and **Roethig** teach the method of claim 15. **Hayashi et al.** teaches a correction step of characterizing, for each cell, the relationship between a drop in voltage and the amount of instantaneous electric current in the form of a table, to thereby correct the amount of instantaneous electric current for each event of the cell (Page 19, CL1, Para 2).

Hayashi et al. does not expressly teach a step of calculating a drop in voltage from the amount of electric current determined according to the type of cell and from the resistance of a power line. **Kuwano et al.** teaches a step of calculating a drop in voltage from the amount of electric current determined according to the type of cell and from the resistance of a power line (CL2, L29-33), as that would allow analyzing the variations in the source voltage of a semiconductor device without test patterns (CL1, L9-10). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Kuwano et al.** that included a step of calculating a drop in voltage from

the amount of electric current determined according to the type of cell and from the resistance of a power line. The artisan would have been motivated because that would allow analyzing the variations in the source voltage of a semiconductor device without test patterns.

12.5 As per Claim 22, **Hayashi et al., Zarkesh et al.** and **Roethig** teach the method of claim 15. **Hayashi et al.** teaches a correction step of characterizing, for each cell, the relationship between a drop in voltage and the amount of instantaneous electric current in the form of a table, to thereby correct the amount of instantaneous electric current for each event of the cell (Page 19, CL1, Para 2).

Hayashi et al. does not expressly teach a step of calculating a drop in voltage from the amount of electric current determined according to the type of cell, the resistance of a power line, and the capacitance of an on-chip capacitor. **Kuwano et al.** teaches a step of calculating a drop in voltage from the amount of electric current determined according to the type of cell, the resistance of a power line, and the capacitance of an on-chip capacitor (CL2, L29-33), as that would allow analyzing the variations in the source voltage of a semiconductor device without test patterns (CL1, L9-10). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Kuwano et al.** that included a step of calculating a drop in voltage from the amount of electric current determined according to the type of cell, the resistance of a power line, and the capacitance of an on-chip capacitor. The artisan would have been motivated because that would allow analyzing the variations in the source voltage of a semiconductor device without test patterns.

12.6 As per Claim 23, **Hayashi et al., Zarkesh et al., Roethig** and **Kuwano et al.** teach the method of claim 10. **Hayashi et al.** teaches that the correction step includes a step of iterating several times calculation of a drop in voltage and correction of a current waveform (Page 19, CL1, Para 3).

13. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hayashi et al.** ("EMI- Noise analysis under ASIC design environment", ACM 1999) in view of **Zarkesh et al.** (U.S. Patent 6,212,665), and further in view of **Roethig** (U.S. Patent 5,835,380) and **Schaefer** (U.S. Patent 5,617,325).

13.1 As per Claim 12, **Hayashi et al., Zarkesh et al.** and **Roethig** teach the method of claim 1. **Hayashi et al.** teaches that the FFT processing step includes a step of subjecting to FFT processing information concerning a change in current, the information being calculated in the multi-order-function waveform modeling step (Page 19, CL2, Para 3)

Hayashi et al. does not expressly teach that the modeling step includes a multi-order-function waveform modeling step of modeling the instantaneous current as a multi-order-function waveform. **Schaefer** teaches that the modeling step includes a multi-order-function waveform modeling step of modeling the instantaneous current as a multi-order-function waveform (CL6, L2-13) because the step response of a target element can be represented by a multi-order-function, when a voltage step from an initial voltage to a final voltage is applied to the input node of an element (CL6, L5-13). It would have been obvious to

one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Schaefer** that included the modeling step including a multi-order-function waveform modeling step of modeling the instantaneous current as a multi-order-function waveform. The artisan would have been motivated because the step response of a target element could be represented by a multi-order-function, when a voltage step from an initial voltage to a final voltage is applied to the input node of an element.

13.2 As per Claim 13, **Hayashi et al., Zarkesh et al.** and **Roethig** teach the method of claim 1. **Hayashi et al.** teaches that the FFT processing step includes a step of subjecting to FFT processing information concerning a change in current, the information being calculated in the exponential-function waveform modeling step (Page 19, CL2, Para 3)

Hayashi et al. does not expressly teach that the modeling step includes an exponential function waveform modeling step of modeling the instantaneous current as an exponential-function waveform. **Schaefer** teaches that the modeling step includes an exponential function waveform modeling step of modeling the instantaneous current as an exponential-function waveform (Fig. 5; CL5, L42-52), because the exponential waveform models the current that approaches asymptotically the final value as the voltage approaches asymptotically the final value (CL5, 49-50). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Schaefer** that included the modeling step including an exponential function waveform modeling step of modeling the instantaneous current as an exponential-function waveform. The artisan would have been motivated because the exponential waveform would model the current

that approaching asymptotically the final value as the voltage approached asymptotically the final value.

14. Claims 18, 19 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hayashi et al.** ("EMI- Noise analysis under ASIC design environment", ACM 1999) in view of **Zarkesh et al.** (U.S. Patent 6,212,665), and further in view of **Roethig** (U.S. Patent 5,835,380) and **Kamiya et al.** (U.S. Patent 6,304,998).

14.1 As per Claim 18, **Hayashi et al., Zarkesh et al.** and **Roethig** teach the method of claim 15. **Hayashi et al.** does not expressly teach that the calculation step includes a step of setting a plurality of peak currents for a composite cell. **Kamiya et al.** teaches that the calculation step includes a step of setting a plurality of peak currents for a composite cell (Abstract, L1-10; Fig 13; Fig. 31 and 32; CL1, L19-23), because the instantaneous current for the composite cells (macros) comprising a plurality of cells varies depending on the input through rate of the input signal supplied to the input terminal and the load capacitance connected to the output terminal (CL2, L8-12). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Kamiya et al.** that included the calculation step including a step of setting a plurality of peak currents for a composite cell. The artisan would have been motivated because the instantaneous current for the composite cells (macros) comprising a plurality of cells would vary depending on the input through rate of the input signal supplied to the input terminal and the load capacitance connected to the output terminal.

Hayashi et al. does not expressly teach that calculating the heights of a plurality of rectangular waveforms through use of a characterized library, and the rectangular waveform modeling step corresponds to a step of modeling the amount of electric current into a plurality of rectangular waveforms. **Roethig** teaches that calculating the heights of a plurality of rectangular waveforms through use of a characterized library, and the rectangular waveform modeling step corresponds to a step of modeling the amount of electric current into a plurality of rectangular waveforms (Abstract, L1-2 and L7-12; CL3, L25-30; CL5, L13-33; CL6, L17-22; CL3, L23-25), because rectangular waveforms represent the Vdd and Vss currents consumed by the cells (CL5, L28-29); and by decomposing the cell currents, the circuit designer can perform more accurate power analysis and modify the design to better accommodate the power consumption by changing the loading of the cell to reduce the load current (CL3, L16-22); and as per **Hayashi et al.**, by performing fast Fourier transformation for the current waveforms, EMI noise spectrum can be obtained (Page 19, CL2, Para 2 & 3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Roethig** that included calculating the heights of a plurality of rectangular waveforms through use of a characterized library, and the rectangular waveform modeling step corresponding to a step of modeling the amount of electric current into a plurality of rectangular waveforms. The artisan would have been motivated because rectangular waveforms would represent the Vdd and Vss currents consumed by the cells; and by decomposing the cell currents, the circuit designer could perform more accurate power analysis and modify the design to better accommodate the power consumption by changing the loading of the cell to reduce the load

current; and by performing fast Fourier transformation for the current waveforms, EMI noise spectrum could be obtained.

14.2 As per Claim 19, **Hayashi et al., Zarkesh et al.** and **Roethig** teach the method of claim 15. **Hayashi et al.** does not expressly teach that the calculation step includes a step of setting a plurality of peak currents for each of the rise and fall of a flip-flop (FF) cell. **Kamiya et al.** teaches that the calculation step includes a step of setting a plurality of peak currents for each of the rise and fall of a flip-flop (FF) cell (Abstract, L1-10; Fig 13; Fig. 31 and 32; CL1, L19-23), because the instantaneous current for the composite cells (macros) comprising a plurality of cells varies depending on the input through rate of the input signal supplied to the input terminal and the load capacitance connected to the output terminal (CL2, L8-12). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Kamiya et al.** that included the calculation step including a step of setting a plurality of peak currents for each of the rise and fall of a flip-flop (FF) cell. The artisan would have been motivated because the instantaneous current for the composite cells (macros) comprising a plurality of cells would vary depending on the input through rate of the input signal supplied to the input terminal and the load capacitance connected to the output terminal.

Hayashi et al. does not expressly teach that calculating the heights of a plurality of rectangular waveforms through use of a characterized library, and the rectangular waveform modeling step corresponds to a step of modeling the amount of electric current into a plurality of rectangular waveforms. **Roethig** teaches that calculating the heights of a plurality of rectangular

waveforms through use of a characterized library, and the rectangular waveform modeling step corresponds to a step of modeling the amount of electric current into a plurality of rectangular waveforms (Abstract, L1-2 and L7-12; CL3, L25-30; CL5, L13-33; CL6, L17-22; CL3, L23-25), because rectangular waveforms represent the Vdd and Vss currents consumed by the cells (CL5, L28-29); and by decomposing the cell currents, the circuit designer can perform more accurate power analysis and modify the design to better accommodate the power consumption by changing the loading of the cell to reduce the load current (CL3, L16-22); and as per **Hayashi et al.**, by performing fast Fourier transformation for the current waveforms, EMI noise spectrum can be obtained (Page 19, CL2, Para 2 & 3). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Roethig** that included calculating the heights of a plurality of rectangular waveforms through use of a characterized library, and the rectangular waveform modeling step corresponding to a step of modeling the amount of electric current into a plurality of rectangular waveforms. The artisan would have been motivated because rectangular waveforms would represent the Vdd and Vss currents consumed by the cells; and by decomposing the cell currents, the circuit designer could perform more accurate power analysis and modify the design to better accommodate the power consumption by changing the loading of the cell to reduce the load current; and by performing fast Fourier transformation for the current waveforms, EMI noise spectrum could be obtained.

14.3 As per Claim 27, **Hayashi et al., Zarkesh et al.** and **Roethig** teach the method of claim 1. **Hayashi et al.** teaches a triangular waveform modeling step of modeling the amount of

instantaneous electric current as a plurality of triangular waveforms through use of a table representing the relationship between the width and height of a triangular waveform (Page 19, CL1, Para 1; Fig 10; Page 18, CL2, Para 4); and the FFT processing step includes a step of subjecting to FFT processing information concerning a change in current, the information being calculated in the triangular waveform modeling step (Page 19, CL2, Para 3).

Hayashi et al. does not expressly teach that the modeling step includes a step of calculating the amount of instantaneous electric current from each event information in the case of a composite cell. **Kamiya et al.** teaches that the modeling step includes a step of calculating the amount of instantaneous electric current from each event information in the case of a composite cell (Abstract, L1-10; Fig 13; Fig. 31 and 32; CL1, L19-23), because the instantaneous current for the composite cells (macros) comprising a plurality of cells varies depending on the input through rate of the input signal supplied to the input terminal and the load capacitance connected to the output terminal (CL2, L8-12). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Hayashi et al.** with the method of **Kamiya et al.** that included the modeling step including a step of calculating the amount of instantaneous electric current from each event information in the case of a composite cell. The artisan would have been motivated because the instantaneous current for the composite cells (macros) comprising a plurality of cells would vary depending on the input through rate of the input signal supplied to the input terminal and the load capacitance connected to the output terminal.

Arguments

15. As per the applicant's arguments, the applicants' attention is requested to the corresponding claim rejections. In addition, the following explanation is provided to further explain the examiner's position.

15.1 As per the Applicant's argument that "Claim 1 was again rejected under 35 U.S.C. §112, second paragraph for being incomplete. Again, applicant does not understand the Examiner's rejection; it again appears that the Examiner wants applicant to add additional steps to the claim; Applicant notes that all of the steps of the claim are part of a method for "analyzing the amount of electromagnetic interference arising in an LSI by means of performing a gate level simulation" as stated in the preamble, and thus no such step as recommended by the Examiner is necessary for completeness....it is enough that the applicant disclose only that which the applicant regards as the invention according to that particular claim; ...Applicant is allowed to specify claims in varying scope", the Examiner respectfully disagrees. The preamble of claim 1 states, "An electromagnetic interference analysis method for analyzing the amount of electromagnetic interference arising in an LSI by means of performing a gate level simulation". Therefore, a step of electromagnetic interference analysis must follow the FFT processing step, to achieve the objective of the preamble.

15.2 As per the applicant's argument that "**Hayashi** teaches only a simplification model for an electric source mesh; **Hayashi** does not disclose a concrete method to analyze EMI by a

gate-level simulation… **Hayashi** presupposes a realization at the transistor level, and discloses only the possibility of applying a gate-level simulation to the EMI analysis, but does not teach any such procedure (and thus is not enabling). The reference teaches only a noise analysis system carried out at the transistor level, and does not teach operability at the gate level. Thus, Hayashi does not enable a gate-level analysis method", the examiner respectfully disagrees.

Hayashi teaches logic simulation using cell switching current waveform library using a netlist as input (Page 18, CL2, Para 3 and 4). The cell simulation includes gate level simulation, since as per **Zarkesh et al.** a cell simulator includes a gate level simulator, since a cell could be a gate (CL1, L40-47). **Hayashi** makes it possible to study the effects caused by LSI currents in the frequency domain (Page 19, CL2, Para 3; FFT transformation permits to study the effects caused by LSI currents in the frequency domain). **Hayashi** does not anywhere state that his simulation is at transistor level or his noise analysis system is at the transistor level. He only states the cell level simulation and noise analysis system.

15.3 As per the Applicant's argument that "Claims 1 and 28 recite transforming the instantaneous current amount into an instantaneous electric current according to a predetermined rule related to the calculated instantaneous current amount; … Hayashi does not disclose any method to transform an instantaneous current amount into an instantaneous current", the examiner takes the position that there is no support for transforming the instantaneous current amount into an instantaneous electric current according to a predetermined rule related to the calculated instantaneous current amount, anywhere in the specification, as explained in Paragraph 3 above.

15.4 As per the Applicant's argument that "Bonitz discloses only the instance name for all cells. It does not overcome the shortcomings of Hayashi", the examiner has used **Zarkesh et al.** which teaches that a cell simulator includes a gate level simulator.

15.5 As per the Applicant's argument that "The invention discloses a method of transforming an instantaneous current "amount" into an instantaneous current "shape", for example; accordingly, the invention introduces a way to utilize gate-level simulation for EMI analysis; the prior art gate-level simulation cannot be utilized for EMI analysis", the examiner respectfully disagrees.

Hayashi et al. teaches a way to utilize gate-level simulation for EMI analysis (Page 16, CL1, Abstract; Page 16, CL2, Para 4; Page 16, CL2, Para 8, using cell information; Page 17, CL1, Para 1, switch-level simulator; Page 18, CL2, Para 3, input netlist, switching simulator; Para 4, logic simulation, each event, when the cell switches; Page 19, Fig. 12, logic simulation, cell switching; Page 19, CL2, Para 3, SPICE simulation, current/voltage waveforms, FFT transform and noise spectrum analysis). **Zarkesh et al.** teaches that the logic simulation performed by **Hayashi et al.** is gate level simulation and therefore involves an electromagnetic interference analysis method for analyzing the amount of electromagnetic interference arising in an LSI by means of performing a gate level simulation (Abstract, L7; CL1, L41-47), because netlist is a gate-level netlist (Abstract, L7); and the term cell includes transistors, gates such as NAND or OR gate and macro circuit portions such as adder or flip-flop (CL1, L41-47) and therefore, the cell level simulation implies gate-level simulation.

15.6 As per the Applicant's argument that "Chen is directed toward predicting worst-case peak currents, and does not consider EMI noise; Chen treats current waveform to time-axis modeling in only a rough manner; Modeling the current peak is different from the actual current waveform; although Chen and Roething may disclose triangular modeling, the references do not disclose any suggestion to apply triangular modeling to gate-level simulations in order to analyze EMI noise", the examiner has used **Hayashi et al.** which applies triangular modeling to gate-level simulations in order to analyze EMI noise (Fig. 10; Page 19, CL2, Para 2 and Para 3).

15.7 As per the Applicant's argument that "Kuwano does not disclose the method for calculating a drop of voltage for each event (i.e., transition time). Kuwano only discloses the voltage drop for a cell delay; There is, thus, no motivation for using a transition time in Kuwano", the examiner has used **Hayashi et al.** which teaches calculating a drop of voltage for each event (i.e., transition time) (Page 19, CL1, Para 2; Page 18, CL2, Para 4).

15.8 As per the Applicant's argument that "The Examiner has not provided the proper motivation for modifying Hayahsi; it is not proper to merely find a reference teaching a missing limitation and stating that adding that limitation would be "obvious" because it might provide some benefit; the Examiner must show that there is some suggestion or motivation to modify the reference (MPEP §2143.01); The prior art must suggest the desirability of the combination (Id.); and merely listing an advantage of the combination is also not sufficient, as some rationale for combining the references must be found in the references themselves", the examiner takes the

position that he has provided the motivations for combing the references taken from the references themselves in all cases. The exact locations in the references where the motivations are found are indicated in all cases of combining the references.

15.9 As per the Applicant's argument that "the Examiner states that Chen was cited only for using triangular waveforms to calculate the peak current, and not for teaching an EMI method; nothing would motivate one reading Hayashi to add the peak current calculation means of Chen; Chen does not suggest use for an EMI method, and Hayashi does not suggest use of triangular waveforms to calculate peak current; instead, the Examiner merely cites the benefits of Chen as motivation for adding Chen to the primary reference... the Examiner has provided no motivation for combining the features", the examiner respectfully disagrees.

Hayashi et al. applies triangular modeling to gate-level simulations, obtains the current waveforms using the simulations and performs FFT on the waveforms to analyze EMI noise (Fig. 10; Page 19, CL2, Para 2 and Para 3). Chen teaches the method of calculating the average current and deriving the current waveforms using the average current, peak current and cycle time (Page 3, CL1, Para 4 to Page 3, Cl2, Para 4). The motivations for combining Chen with **Hayashi et al.** is that the triangular and trapezoidal current waveforms can be derived by calculating the average current (Chen, Page 3, CL1, Para 3).

Conclusion

ACTION IS FINAL

16. Applicants' amendments necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on 571-272-3716. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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